ABSTRACT:

The integrated circuit comprises lateral isolation regions formed at the sides of at least one projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer (402), which is in contact with said projecting region (2), and of a larger isolation layer (411), and it further comprises a zone (5) including a metal silicide situated in the upper part of the polysilicon region (2). Each lateral isolation region comprises a vertical trench (TR) made in the smaller isolation layer (402) between the larger isolation layer (411) and the corresponding side (F) of the projecting region (2), said trench (TR) extending from the top of the larger isolation layer (411) of the corresponding lateral isolation region down to a predetermined depth (h).

Figure 8.